PDTA114EMB

50 V, 100 mA PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

7 February 2023 **Product data sheet**

1. General description

PNP Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC114EMB

2. Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias transistors
- Reduces pick and place costs
- Simplifies circuit design
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm
- AEC-Q101 qualified

3. Applications

- Low-current peripheral driver
- Replaces general-purpose transistors in digital applications
- Control of IC inputs
- Mobile applications

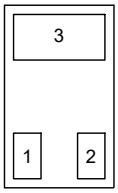
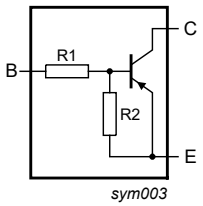
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	-50	V
I_O	output current			-	-	-100	mA
R1	bias resistor 1 (input)	T_{amb} = 25 °C		7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view **DFN1006B-3 (SOT883B)**	
2	G	GND (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA114EMB	DFN1006B-3	plastic, leadless ultra small plastic package; 3 solder lands; 0.35 mm pitch; 1.0 mm x 0.6 mm x 0.37 mm body	SOT883B

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTA114EMB	0001 1001

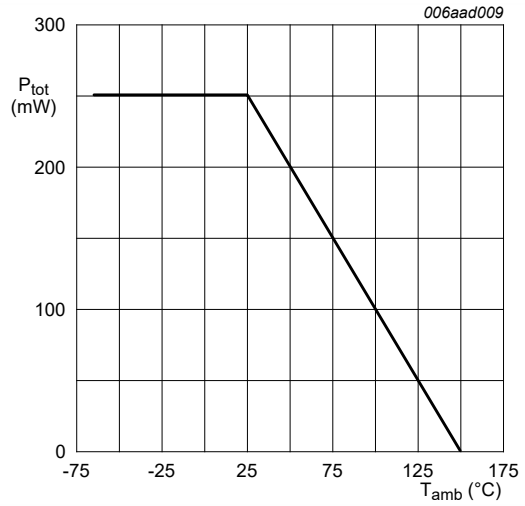
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-10	V
V_I	input voltage			-40	10	V
I_O	output current			-	-100	mA
I_{CM}	peak collector current	$t_p \leq$ 1 ms; pulsed		-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	250	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

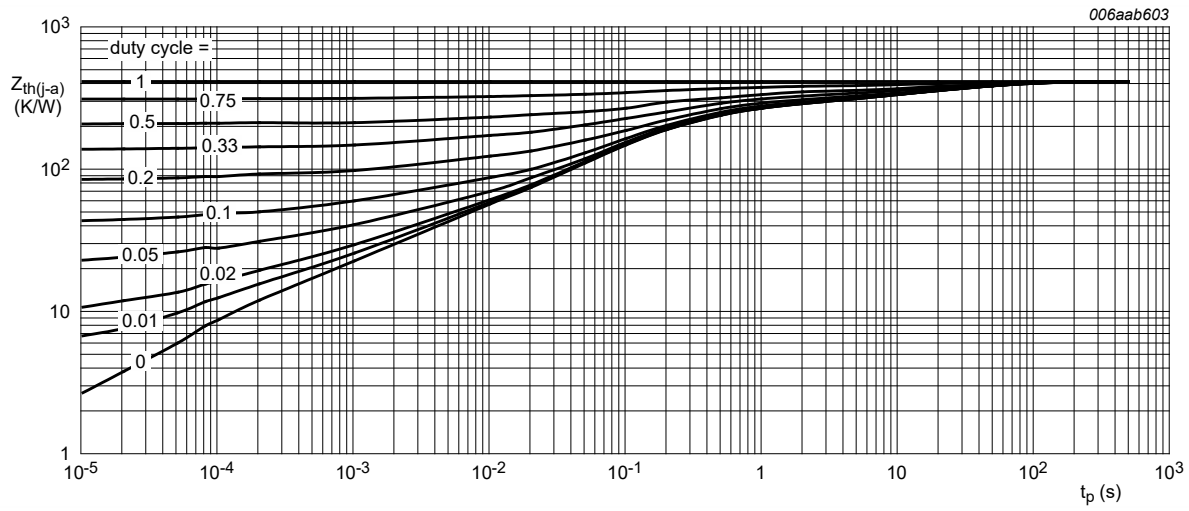
Fig. 1. Power derating curve for DFN1006B-3 (SOT883B)

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

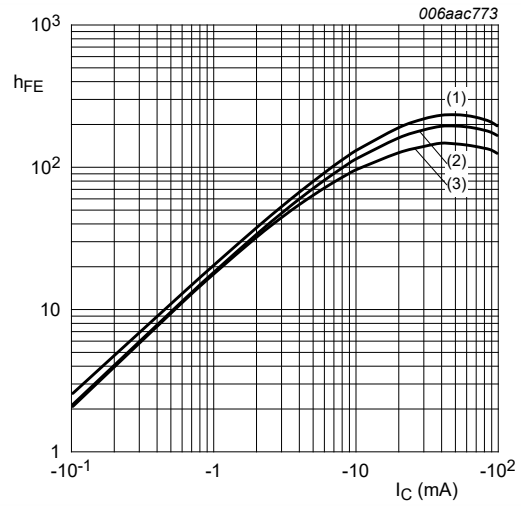
Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

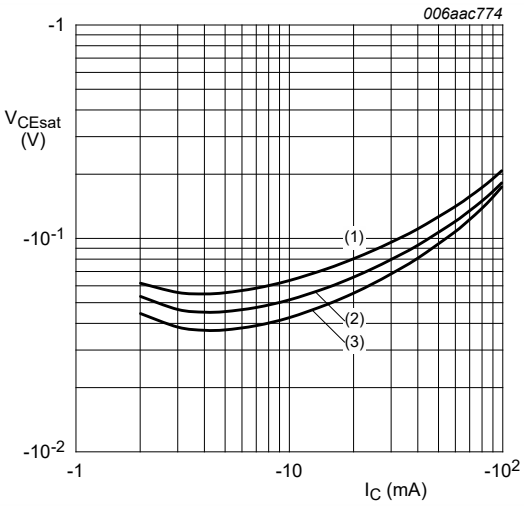
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = -100 µA; I_E = 0 A; T_{amb} = 25 °C		-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = -2 mA; I_B = 0 A; T_{amb} = 25 °C		-50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = -50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = -30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	-1	µA
		V_{CE} = -30 V; I_B = 0 A; T_j = 150 °C		-	-	-5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-400	µA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -5 mA; T_{amb} = 25 °C		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C		-	-	-150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = -5 V; I_C = 100 µA; T_{amb} = 25 °C		-	-1.1	-0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = -0.3 V; I_C = -10 mA; T_{amb} = 25 °C		-2.5	-1.8	-	V
R1	bias resistor 1 (input)	T_{amb} = 25 °C		7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C	[1]	-	180	-	MHz

[1] Characteristics of built-in transistor.



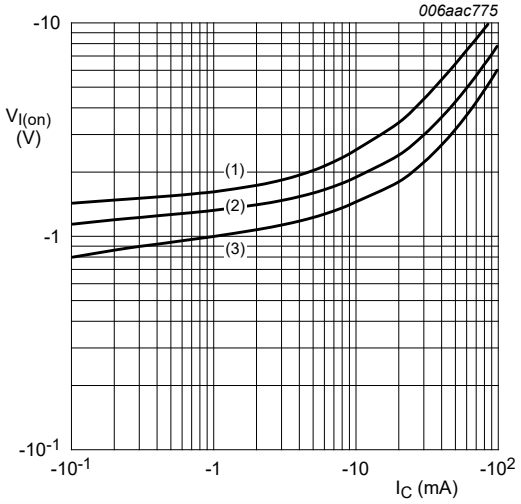
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 3. DC current gain as a function of collector current; typical values



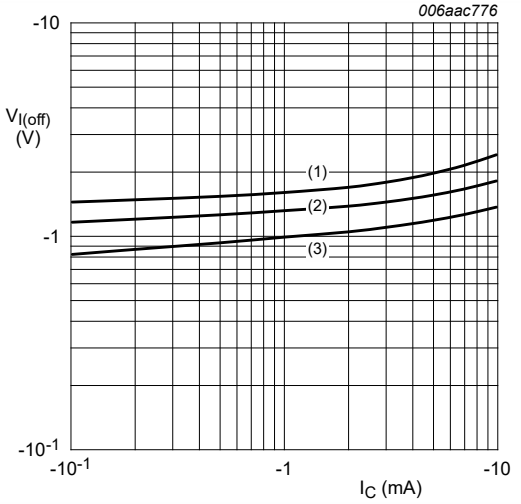
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values



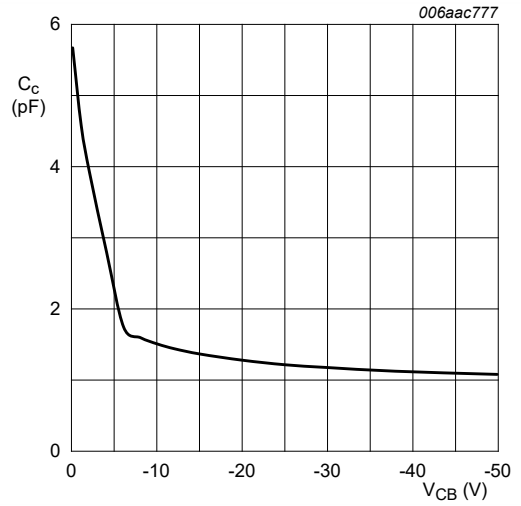
V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector current; typical values



V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 6. Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

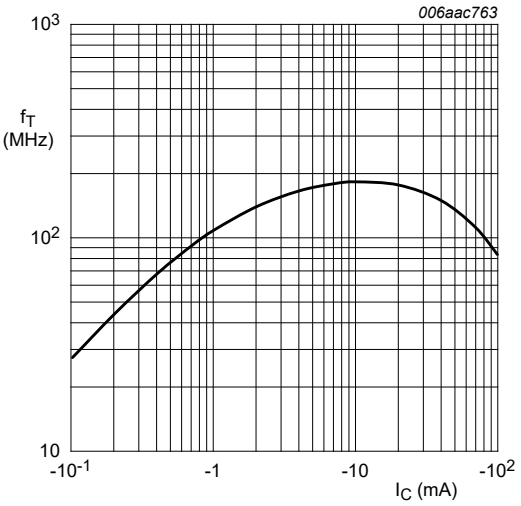


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_3)}{R1 \cdot I_3} - 1$$

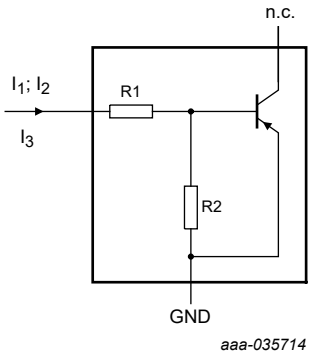


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I_1	I_2	I_3
PDTA114EMB	10	10	-350 µA	-450 µA	400 µA

12. Package outline

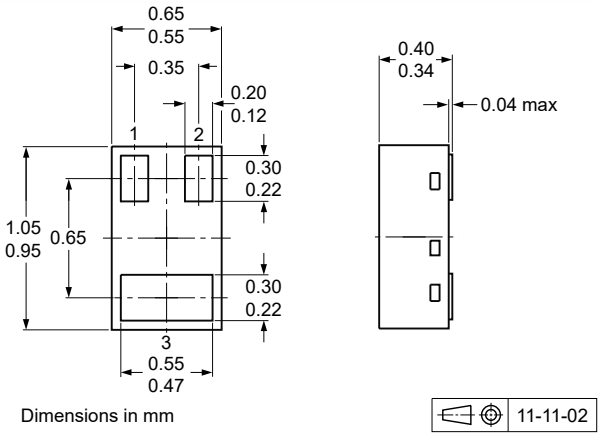


Fig. 10. Package outline DFN1006B-3 (SOT883B)

13. Soldering

Footprint information for reflow soldering of DFN1006B-3 (SOT883B) package **SOT883B**

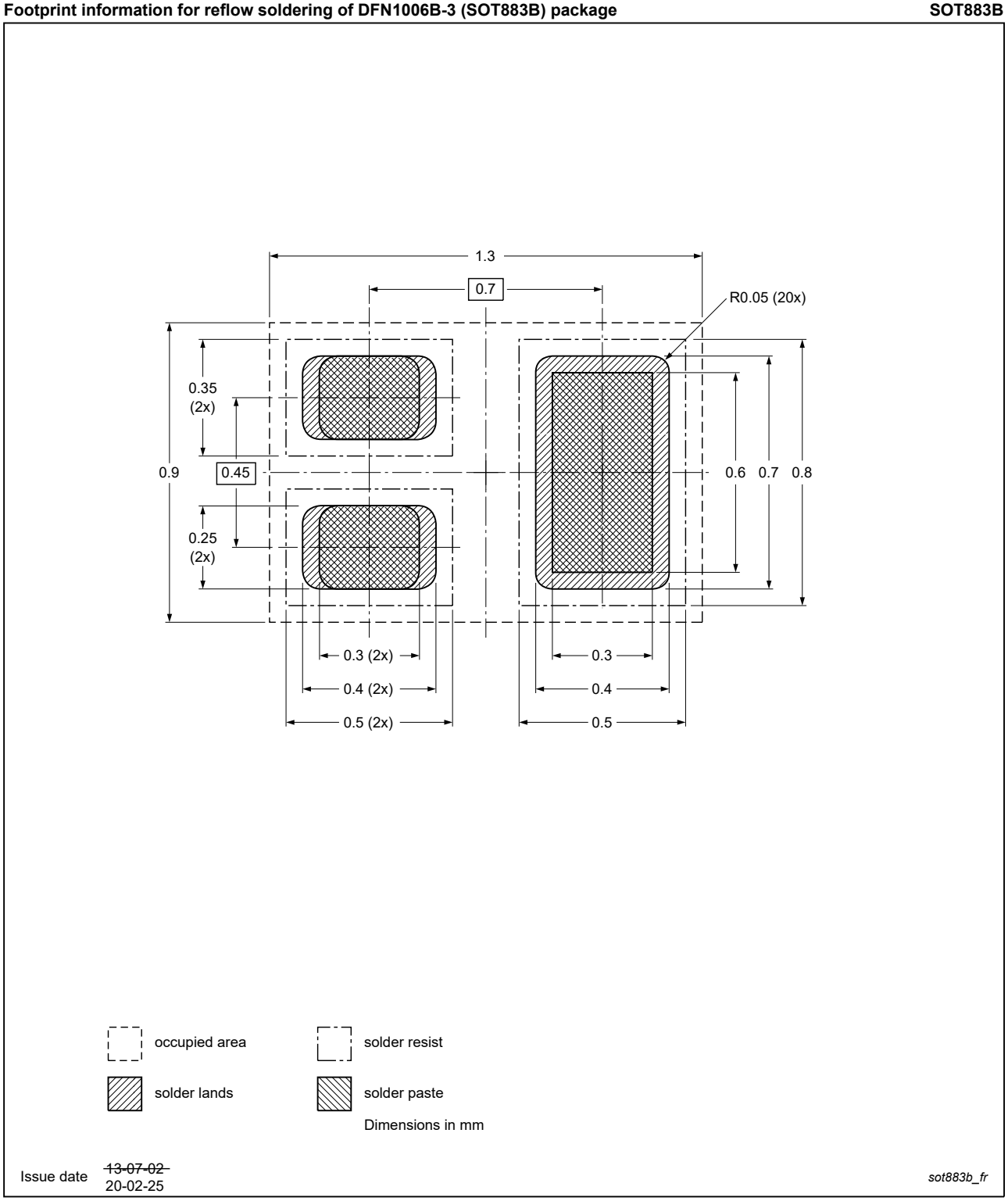


Fig. 11. Reflow soldering footprint for DFN1006B-3 (SOT883B)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA114EMB v.2	20230207	Product data sheet	-	PDTA114EMB v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Limiting values: Values for Input voltage corrected.			
PDTA114EMB v.1	20120515	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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